**OUTPUT WAVEFORMS**

**1.Logic Gates**

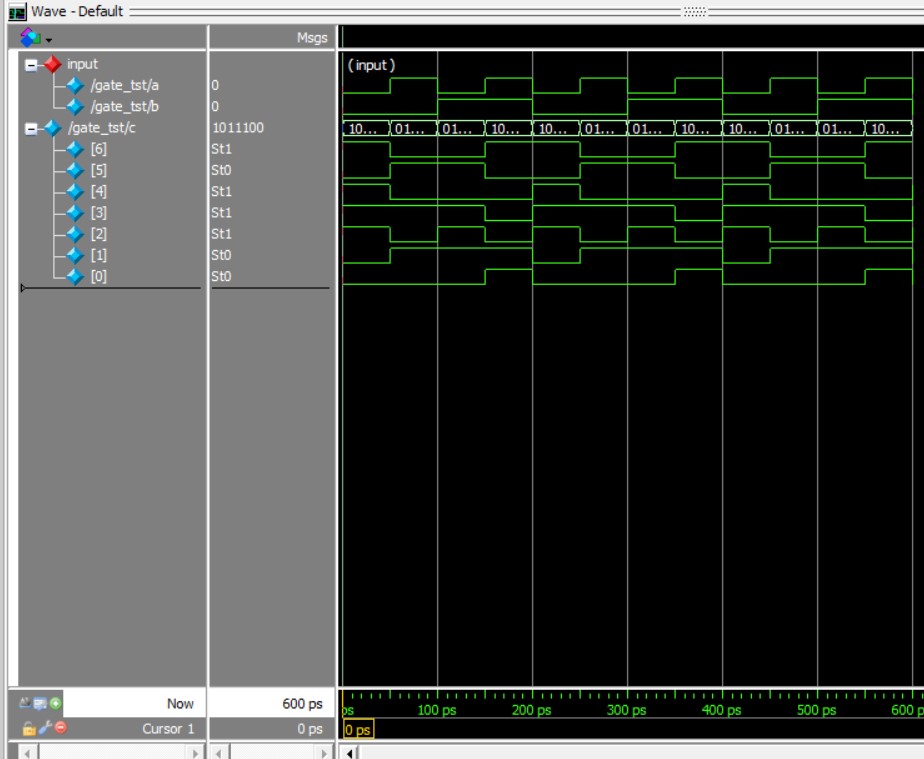
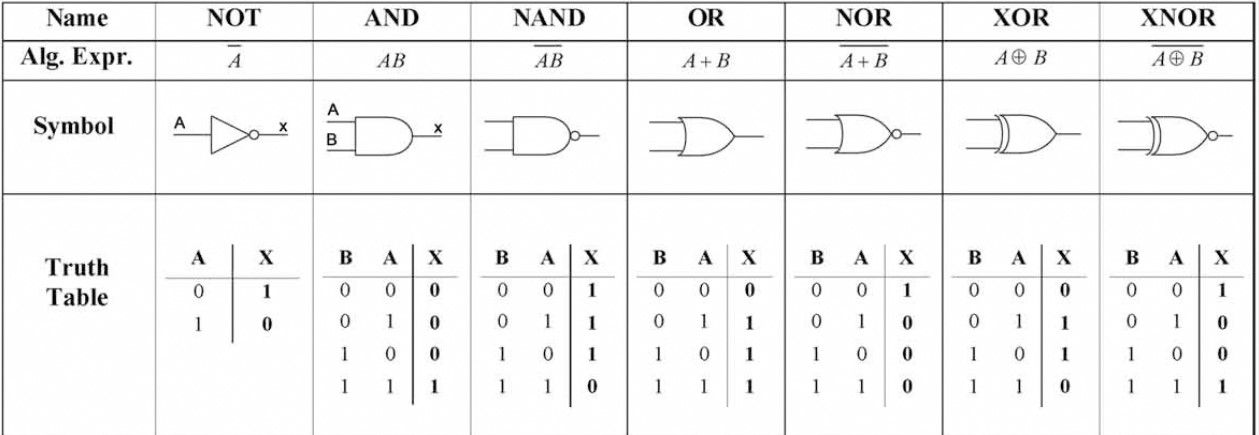


Figure1- **a** and **b** as Input , **c** as Output which include [0]-and gate, [1]-or gate, [2]-not gate, [3]-nand gate, [4]-nor gate, [5]-xor gate, [6]-xnor gate.



**2.Half Adder**

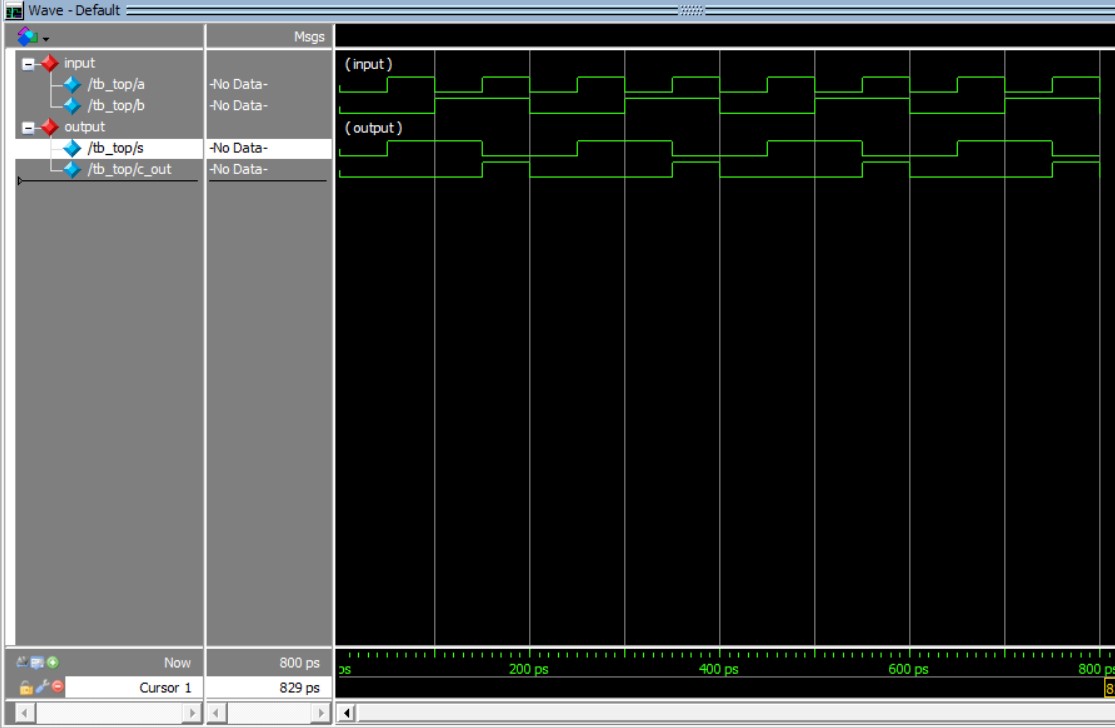
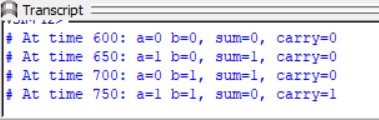


Figure2- **a** and **b** as Input, **s(sum)** and **c\_out(carry)** as Output.



**3.Full Adder**

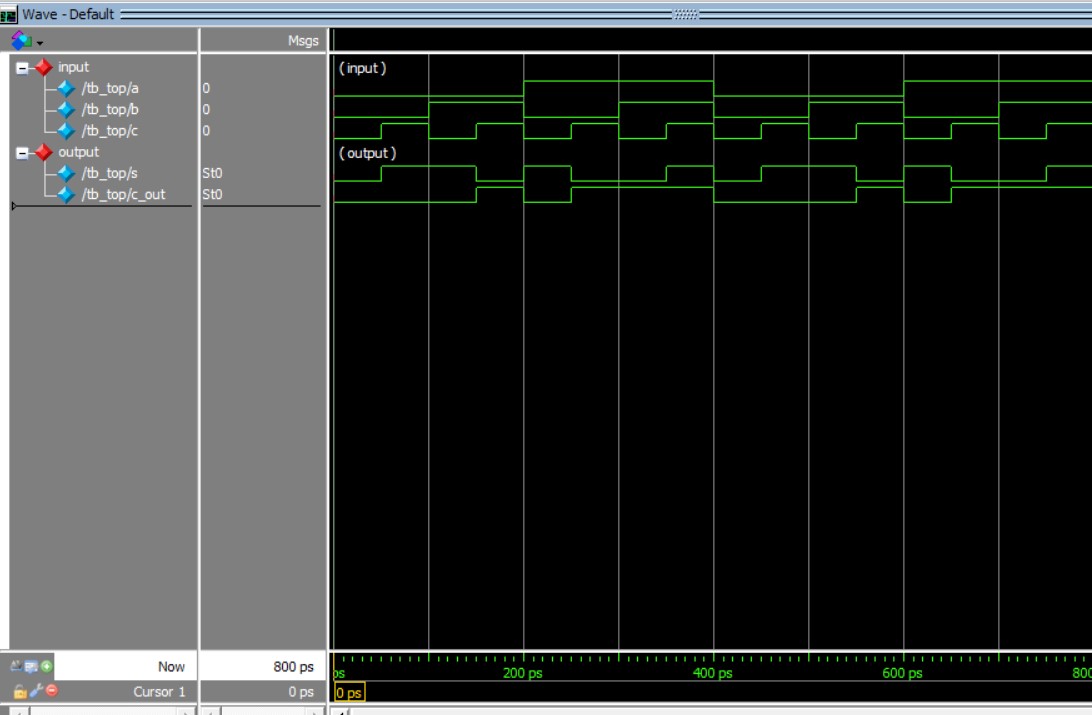
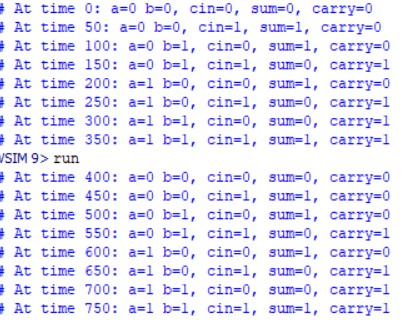


Figure3- **a** and **b, cin** as Input, **s(sum)** and **c\_out(carry)** as Output.



**4.Full Adder using Half Adder**

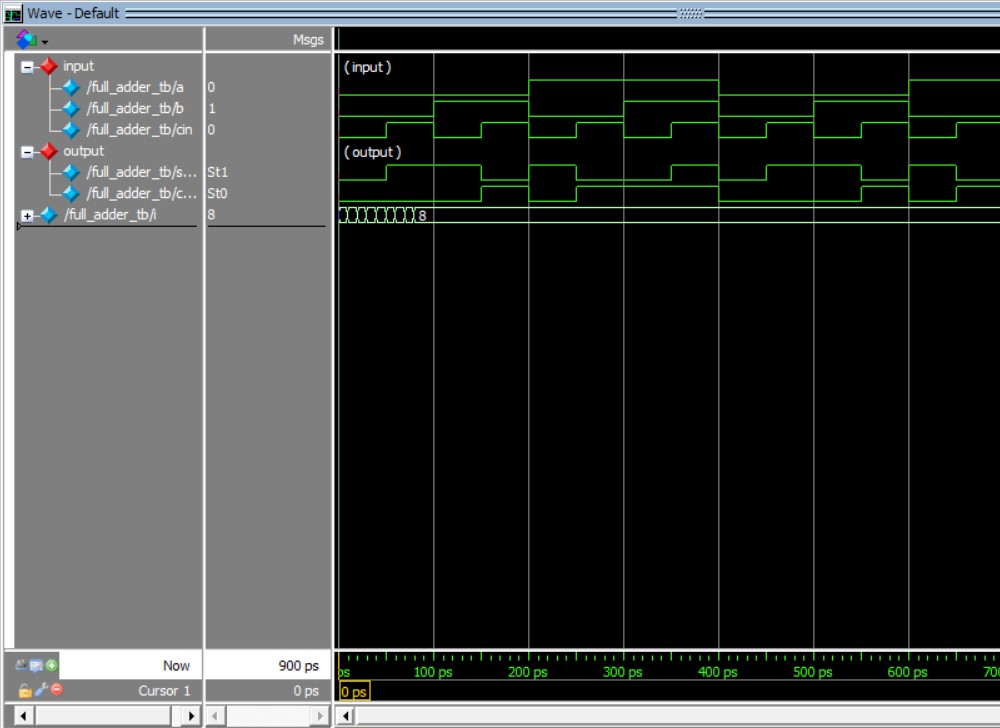
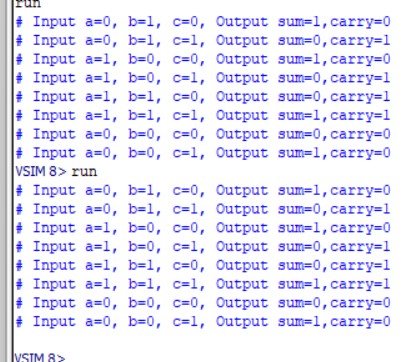


Figure4- **a** and **b, cin** as Input, **s(sum)** and **c\_out(carry)** as Output.



**5.Ripple Carry Adder**

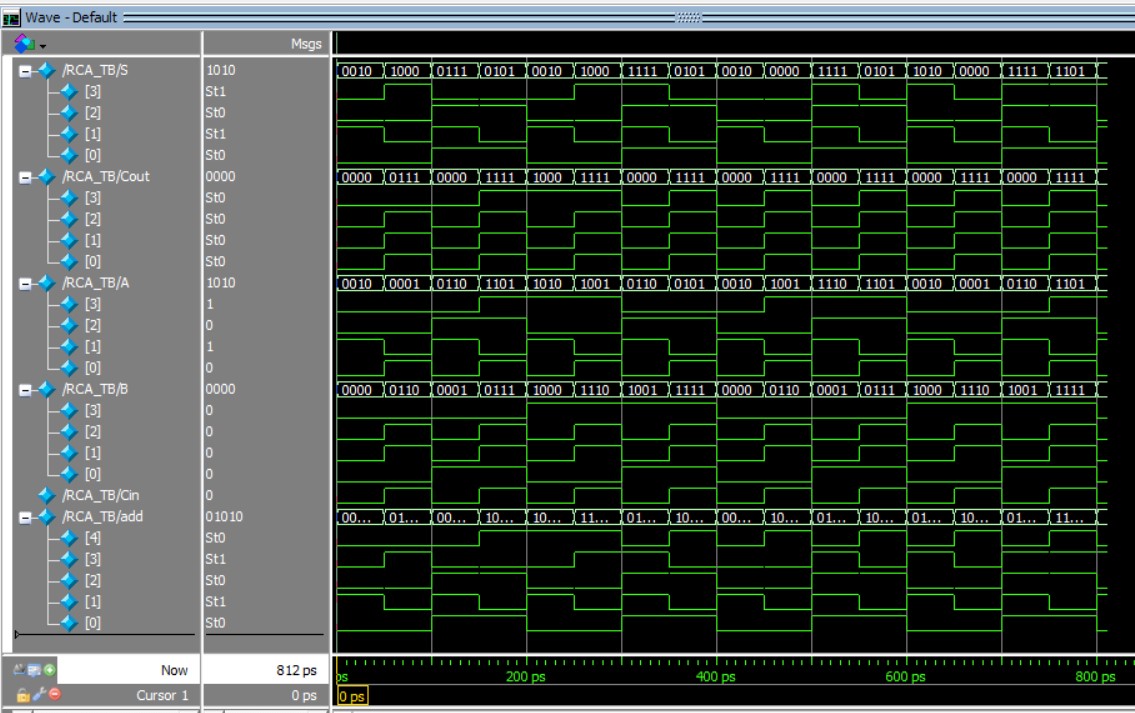
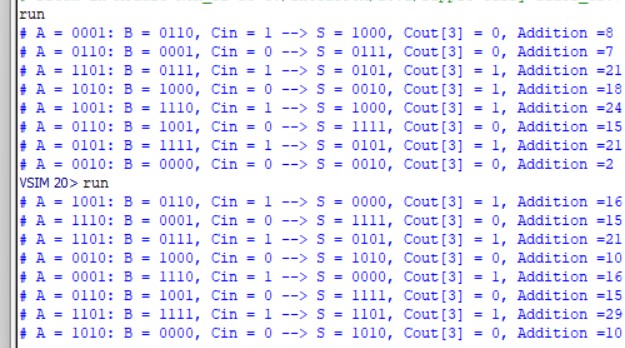


Figure5- **A** and **B, Cin** as Input, **s(sum)** and **Cout(carry), add(addition)** as Output.



**6. 2:1 Multiplexer**

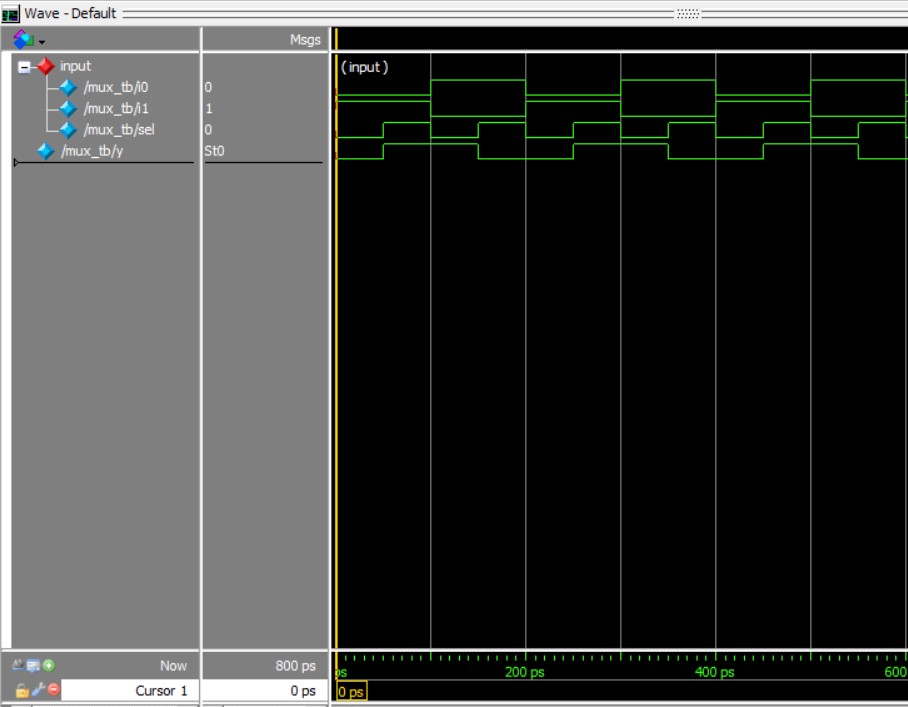
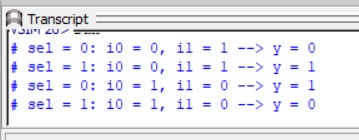


Figure6- **i0** and **i1, sel** as Input, **y** as Output.



**7. 4:1 Multiplexer**

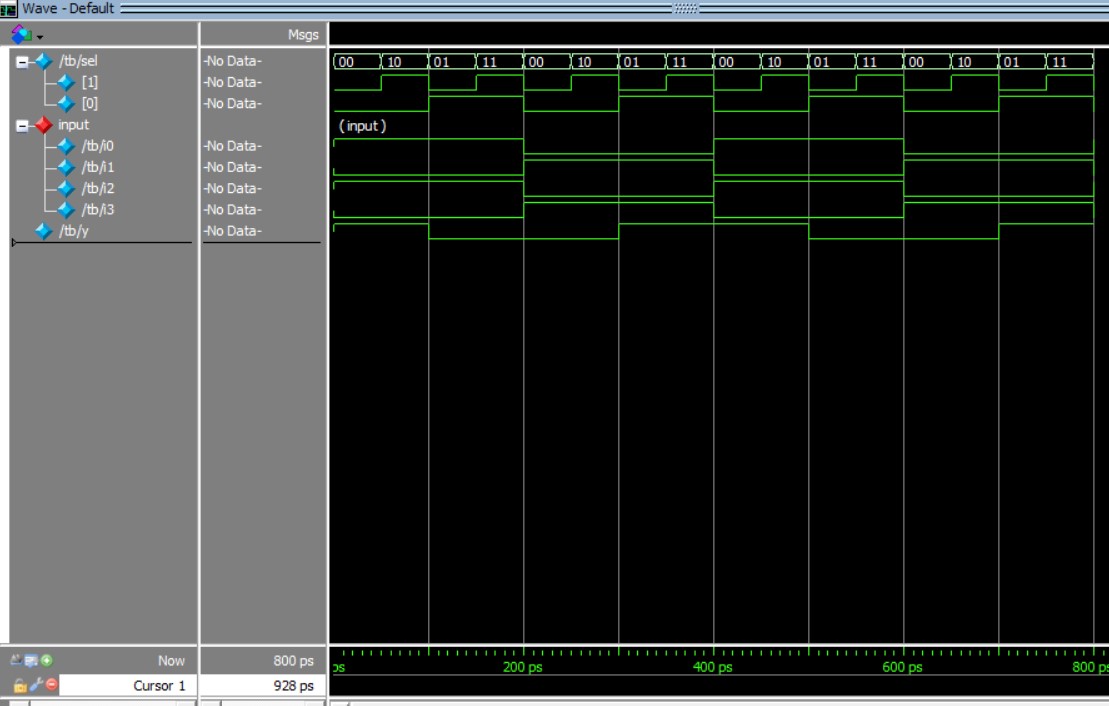


Figure6- **i0, i1, i2** and **i3, sel** as Input, **y** as Output.

